REMARKS

Reconsideration of this application as amended is respectfully requested.

Claims 1, 4, 17, and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Jin et al ("Jin") and the alleged knowledge in the art.

Claims 2, 3, 5, 6, 7, 18, 19, and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Jin in view of Starkovich and Chuang.

Claims 10, 12, 14, 20, and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Papathomas in view of Jin et al.

Applicant reserves all rights with respect to the doctrine of equivalents.

As stated, the Examiner has rejected claims 1, 4, 17 and 22 as being anticipated by Jin. Applicant respectfully submits that Jin does not anticipate claims 1, 4, 17, and 22. Applicant has amended independent claims 1, 4, 17, and 22 to read as follows:

Claim 1 An electronic device comprising:

a substrate having a core, a conductive layer and at least one build up layer disposed on said conductive layer, wherein said substrate is a single unit;

a semiconductor die disposed on said substrate; and

at least one interconnect disposed between the substrate and the semiconductor die, wherein the substrate is bonded to the semiconductor die by the at least one interconnect,

wherein the at least one build up layer comprises at least one binder and at least one filler, and

wherein the at least one filler has a negative coefficient of thermal expansion.

(emphasis added).

Claim 4 A substrate for use in an electronic device, comprising:

a core;

at least one conductive layer disposed on said core;

at least one build up layer having at least one binder and at least one filler disposed on said conductive layer, wherein the at least one filler has a negative coefficient of thermal expansion and wherein said substrate is a single unit.

(emphasis added).

Claim 17 An electronic system comprising:

an electronic device having a substrate, the substrate having a core, and at least one build up layer and at least one conductive layer disposed on the exterior of said core and wherein said substrate is a single unit; and wherein the build up layer comprises at least one binder and at least one filler, wherein the at least one filler has a negative coefficient of thermal expansion.

(emphasis added).

Claim 22 A method of making an electronic device comprising:

providing a substrate having at least one build up layer having a core, a conductive layer, and at least one build up layer disposed on said core, and wherein said substrate is a single unit;

providing a semiconductor die, and

forming at least one interconnect disposed between the substrate and the semiconductor

die, wherein the substrate is bonded with the semiconductor die by the at least one interconnect, wherein the at least one build up layer comprises at least one binder and at least one filler, and wherein the at least one filler has a negative coefficient of thermal expansion.

(emphasis added).

It is respectfully submitted that Jin neither teaches nor suggests a combination with the alleged knowledge in the art. Applicant respectfully submits that Jin discloses a method of reducing the CTE mismatch between a heat sink and a semiconductor substrate to increase the reliability of electronic devices by employing negative CTE bodies in the composite heat sink structure. However, applicant claims a single-unit substrate within an electronic device, along with its method of fabrication, having a core on which a conductive layer and a build up layer are disposed upon. Applicant's claimed invention differs from Jin in that applicant claims a single-unit substrate that includes a build up layer which may have a lower fraction filler loading, to exhibit improved rheological properties, and thus enable improved substrate designs. Applicant teaches that substrates, with build up layers disposed upon, may be designed with smaller features than would otherwise be used with previously known dielectric materials. Therefore, applicant respectfully submits that Jin teaches away from applicant's claimed invention because Jin's method to reduce the CTE mis-match in electronic devices involves an insertion of negative CTE bodies in a heat sink and fails to disclose a single-unit substrate having a core on which a conductive layer and a build up layer is disposed upon within an electronic device.

Applicant respectfully submits that the Examiner's reference of Jin in conjunction with the alleged knowledge in the art is impermissible hindsight based on applicant's own disclosure. Applicant respectfully submits that Jin's disclosure only shows inserting negative CTE bodies in a heat sink within an electronic device.

Applicant respectfully submits that Jin and the alleged knowledge in the art, even if combined, fails to disclose applicant's claimed invention of a substrate within an electronic device, along with its method of fabrication, having a core on which a

conductive layer and a build up layer are disposed upon. It is the Examiner's position that Jin shows in **Figure 7** a **substrate 61** formed of a build up layer comprising at least one binder and at least one filler having a negative coefficient of expansion embedded within. It is also the Examiner's position that **chip 63** of **Figure 7** shows the at least one **interconnect 64** disposed between the substrate and the die. Applicant respectfully disagrees.

First, applicant claims a substrate comprising a core, at least one conductive layer disposed on said core, and at least one build up layer, including a binder and a filler having a negative CTE, disposed on a conductive layer. Applicant respectfully submits that Jin fails to disclose the claimed invention because Jin's disclosure of a heat sink with embedded negative CTE bodies is not equivalent to applicant's substrate having at least one build up layer with a negative CTE filler embedded therein. Applicant further submits that Jin's disclosure of **negative CTE bodies 22** are not equivalent to a build up layer. As claimed, a build up layer is disposed on a conductive layer, which is disposed on the core within a single-unit substrate. In contrast, Jin's negative **CTE bodies 22** are embedded within **heat sink 61**, without being disposed on a conductive layer. Applicants therefore respectfully submits that Jin in view of the alleged knowledge in the art fails to discloses the claimed invention of a single-unit substrate within an electronic device, and its method of fabrication, having a core on which a conductive layer and a build up layer are disposed upon.

Given that claims 2-3, 5-6, 18-19, and 23 are dependent claims that depend directly or indirectly from independent claims 1, 4, 17, and 22 and add additional limitations, it is respectfully submitted that claims 2-3, 5-6, 18-19, and 23 are not unpatentable under 35 U.S.C. §103(a).

As stated, the Examiner has rejected claim 7 under 35 U.S.C. §103(a) in view of Jin, Starkovich, and Chuang. Applicant submits that claim 7 is not obvious under 35 U.S.C §103(a) in view of Jin, Starkovich, and Chuang. Applicant has amended independent claims 7 to read as follows:

Claim 7 A material for use as a build up dielectric layer for a substrate, comprising:
at least one binder;

at least one filler, wherein the at least one filler comprises zirconium tungstate and wherein the zirconium tungstate is a crystalline compound having a nearly isotropic coefficient of thermal expansion of approximately -4.9ppm/degree C or less over the temperature range of -50 degrees C to +250 degrees C.

It is respectfully submitted that Jin, Starkovich, and Chuang neither teaches nor suggests the combination with each other. Applicant respectfully submits that Jin discloses a method of reducing the CTE mismatch between a heat sink and a semiconductor substrate, to increase the reliability of electronic devices, by employing negative CTE bodies in the composite heat sink structure. Applicant further submits that Starkovich discloses a filled composite composition that can be used as adhesives, encapsulants, underfill materials, and potting materials in electronic packages and that Chuang discloses a low-CTE packaging material for assembling a semiconductor die into a package. Applicant respectfully submits that the combination of Jin, Starkovich, and Chuang might provide a means of forming an electronic package including CTE compatible encapsulants, underfills, adhesives, and potting materials. Applicant submits that in relation to advanced electronic packages, which include substrates that comprise a core, build up layer, and conductive layers, the combination of Jin, Starkovich, and Chuang would not be suggested primarily because a material to be used in a build up layer is not disclosed in the cited prior art references. Therefore, applicant respectfully submits that Jin, in view of Starkovich and Chuang, teaches away from applicant's claimed invention.

Applicant respectfully submits that the Examiner's refernce of Jin in conjunction with Starkovich and Chuang is impermissible hindsight based on applicant's own disclosure. Applicant submits that Jin, in view of Starkovich and Chuang, only shows adding negative CTE materials to encapsulants, underfills, adhesives, and potting materials within an electronic package, but not within a build up dielectric material for a substrate.

Applicant respectfully submits that Jin, Starkovich, and Chuang, even if combined, fail to disclose applicant's claimed invention of a material for use as a build up dielectric layer for a substrate. It is the Examiner's position that the term "build up" layer

fails to be specifically defined in the claims, fails to have a special meaning that would limit the structure of the layer, and is not established to have any well known meaning in the art, and therefore the term "build up" layer is being considered to have an obvious meaning as a "layer of material" or "material structure" in the broadest sense. It is also the Examiner's position that although Jin fails to specifically mention the use of a filler comprising zirconium tungstate, Starkovich and Chuang, however, discloses a filler comprising zirconium tungstate. Applicant respectfully disagrees.

First, applicant submits that neither Jin, Starkovich, nor Chuang discloses a material for use as a build up dielectric layer. Jin discloses a thin layer of an epoxy or solder; Starkovich discloses an adhesive, encapsulant, underfill, and potting material; and Chuang discloses a low CTE attach material (underfill) and a low CTE lid. Applicant submits that neither an epoxy, solder, adhesive, encapsulant, underfill, potting material, low CTE attach material, nor a low CTE lid is equivalent to a build up layer as taught and claimed by applicant. Furthermore, applicant submits that even if the combination of Starkovich and Chuang discloses a filler comprising zirconium tungstate, the combination in light with Jin is moot because the cited art fails to disclose said filler in a build up layer. Therefore, applicant submits that Jin, in view of Starkovich and Chuang, fails to disclose the claimed invention of a material for use as a build up dielectric layer for a substrate.

As stated, the Examiner has rejected claims 10, 14, and 20 under 35 U.S.C. §103(a) as unpatentable over Papathomas in view of Jin. Applicant respectfully submits that Papathomas does not anticipate claims 10, 14, and 20. Applicant has amended independent claims 10, 14, and 20 to read as follows:

Claim 10 An electronic device comprising:

a semiconductor die,

a next level package <u>having a core, a conductive layer and an at least one build up layer disposed on the exterior of said conductive layer, wherein said next level package is a single unit;</u>

an at least one interconnect disposed between the semiconductor die and

the next level package, and

an underfill disposed at least in part between the semiconductor die and the next level package, and wherein the semiconductor die is bonded to the next level package by the at least one interconnect, and wherein the semiconductor die is bonded to the next level package by the underfill, wherein the underfill comprises at least one binder and at least one filler, and wherein the at least one filler comprises zirconium tungstate; and wherein the zirconium tungstate is a crystalline compound having a nearly isotropic coefficient of thermal expansion of approximately -4.9ppm/degree C or less over the temperature range of -50 degrees C to +250 degrees C.

(emphasis added).

Claim 14 A method of bonding a semiconductor die to ~~with~~ a next level package, comprising:

providing at least one interconnect;

providing an underfill material having at least one binder and at least one filler, wherein the at least one filler comprises zirconium tungstate; wherein the zirconium tungstate is a crystalline compound having a nearly isotropic coefficient of thermal expansion of approximately -4.9ppm /degree C or less over the temperature range of -50 degrees C to +250 degrees C;

arranging the semiconductor die, the next level package, the at least one interconnect and the underfill material such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die with the next level package and such that the underfill material is disposed at least in part between the semiconductor die and the next level package; wherein said next level package comprises a core, a conductive

layer, and at least one build up layer disposed on the exterior of said conductive layer and wherein said next level package is a single unit;

causing the at least one interconnect to bond the semiconductor die with the next level package; and

causing the underfill material to bond the semiconductor die with the next level package.

(emphasis added).

Claim 20: An electronic system comprising:

an electronic device having a semiconductor die bonded ~~with~~ to a next level package by an underfill disposed at least in part between the semiconductor die and the next level package, wherein the next level package comprises a core, a conductive layer and at least one build up layer disposed on the exterior of said conductive layer and wherein said next level package is a single unit;

wherein the underfill and the build up layer comprises at least one binder and at least one filler, and wherein the at least one filler comprises crystalline zirconium tungstate having a nearly isotropic coefficient of thermal expansion of approximately -4.9ppm/degree C or less over the temperature range of -50 degrees C to +250 degrees C.

(emphasis added).

It is respectfully submitted that Papathomas and Jin neither teaches nor suggests a combination with each other. Applicant respectfully submits that Papathomas discloses an encapsulant (underfill) composition comprising a resin material, a flexibilizing agent, and a filler material in the manufacture of a chip carrier usable as part of an electronic package. Applicant submits that Jin discloses a method of reducing the CTE mismatch between a heat sink and a semiconductor substrate to increase the reliability of electronic

devices by employing negative CTE bodies in the composite heat sink structure. Applicant, however, claims an electronic device that includes a single-unit next level package having a core, a conductive layer, and an at least one build up layer disposed on the conductive layer (claim 10), a method of bonding a semiconductor die to a single-unit next level package wherein the next level package comprises a core, a conductive layer, and at least one build up layer disposed on the conductive layer (claim 14), and an electronic system which includes a next level package comprising a core, a conductive layer, and at least one build up layer disposed on the conductive layer (claim 20). Applicant submits that applicant's claimed invention differs from Papathomas and Jin in that applicant claims a next level package that includes a build up layer which may have a lower fraction filler loading to exhibit improved rheological properties and thus enable improved substrate designs. Applicant teaches that next level packages with build up layers disposed upon may be designed with smaller features than would otherwise be used with previously known dielectric materials. Applicant respectfully submits that Papathomas teaches away from applicant's claimed invention because Papathomas' disclosure of an encapsulant composition as part of an electronic package in view of Jin's disclosure of a method of reducing the CTE mismatch between a heat sink and a semiconductor substrate involves an insertion of negative CTE bodies in an encapsulant and fails to disclose a build up layer disposed upon a core within an electronic device or within an electronic system.

Applicant respectfully submits that the Examiner's reference of Papathomas in conjunction with Jin is impermissible hindsight based on applicant's own disclosure. Papathomas only discloses inserting negative CTE bodies in an encapsulant for use within an electronic package.

Applicant respectfully submits that Papathomas and the Jin, even if combined, fail to disclose applicant's claimed invention of a an electronic device that includes a single-unit next level package having a core and an at least one build up layer disposed on the exterior of the core (claim 10), a method of bonding a semiconductor die to a next level package wherein the single-unit next level package comprises a core, a conductive layer, and at least one build up layer disposed on the conductive layer (claim 14), and an electronic system which includes a single-unit next level package comprising a core, a

conductive layer, and at least one build up layer disposed on the conductive layer (claim 20). It is the Examiner's position that Papathomas shows in **Figure 1** an electronic device having a **die 6** bonded to a next level package (substrate 2), and at least one interconnect (i.e. solder balls and pads-not labeled) are shown disposed between the die and the next level package. The Examiner further posits that an underfill 14 is disposed at least in part between the die and the next level package and comprises at least one binder and at least one filler (i.e. zirconium tungstate); wherein the die is shown bonded to the next level package by the interconnect and underfill. Furthermore, the Examiner maintains that Jin teaches the use of a negative CTE filler material having the characteristics recited in claim 20. Applicant respectfully disagrees.

Applicant respectfully submits that Papathomas in view of Jin fails to disclose the claimed invention because Papathomas' disclosure of an **encapsulant 14** (underfill) disposed on a **substrate 2** is not equivalent to applicant's single-unit next level package having a core, a conductive layer, and at least one build up layer with a negative CTE filler embedded therein. Moreover, applicant's claim of a single-unit next level package having a core, a conductive layer, and a build up layer is distinguishable from Papathomas' disclosure of an encapsulant (underfill) because applicant's build up layer is contained within a substrate as a single unit contrary to Papathomas' distinct encapsulant (underfill) and substrate components. Applicant therefore submits that Papathomas, in view of Jin, fails to disclose the claimed invention of an electronic device that includes a single-unit next level package having a core, a conductive layer, and an at least one build up layer disposed on the conductive layer (claim 10), a method of bonding a semiconductor die to a single-unit next level package wherein the next level package comprises a core, a conductive layer, and at least one build up layer disposed on the conductive layer (claim 14), and an electronic system which includes a single-unit next level package comprising a core, a conductive layer, and at least one build up layer disposed on the conductive layer (claim 20).

Given that claims 12 and 21 are dependent claims that depend directly or indirectly from independent claims 10, 14, and 20 and add additional limitations, it is respectfully submitted that claims 12 and 21 are not unpatentable under 35 U.S.C. §103(a).

Applicants respectfully submit that the applicable rejections and objections have been overcome. Favorable action is respectfully solicited.

If there are any additional charges, please charge Deposit Account # 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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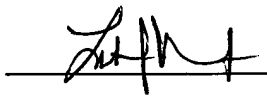

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